**Chapter 1**

**Introduction**

* 1. **Motivation**Microelectronic products continue to connect and change to control our world in the 21st century thanks to unprecedented technological advances and rapid adoption in economic and industrial society. In addition to the successful parade of smartphones contemporary achievements such as activity trackers delivery drones and electric vehicles as well as bio-implants for driverless cars and ongoing innovations related to the Internet of Things will not only address many logistical and medical and environmental problems of Today. but they have profoundly revolutionized modern life in many respects.   
     Driven by a market demand for low-cost, multi-purpose, and densely integrated circuits (ICs), the semiconductor industry can be seen to follow a trend towards system-on-chip (SOC) solutions with a growing amount of mixed-signal content, i.e., both digital and analog IC sections. Due to the growing need for more computing power digital circuits have long been of great interest but now analog circuits are also of great interest. , primarily incited by the desire for functional diversification and system integration. Amongst others, the soaring importance of sensor functionality and the sophistication of advanced human-machine interfaces make Analog circuit parts are more important

Increasing chip complexity and shortening product lifecycles require electronic design automation in both the digital and analog domains to complete the task of creating IC designs. But even digital IC design follows a highly automated algorithm synthesis flow from the start. Analog circuits are typically produced by experienced designers with a low level of automation especially since the schematic design phase where the circuit diagram is converted to the actual implementation circuit is a major bottleneck in the overall design flow Figure( 1.1).

Figure 1.1: Simplified illustration of the integrated circuit design flow.


Topic of this Thesis

+ **Automation**

Figure 1. 1: Simplified illustration of the integrated circuit design flow.

The task of verifying the system specification as an electronic circuit is a very creative act. This is especially true for the analog layout design steps that this paper focuses on. Analog layout design relies heavily on the intuitive experience and creativity of the designers involved and is therefore considered an art by many experts in the field. This is also reflected in Alan Hastings title The Art of Analog Layout [[[1]](#footnote-1)] . It is considered standard work in the analog display community. Unfortunately these human characteristics cannot be easily automated on a scale that meets industrial needs.

In the past, layout design was done manually using drafting tools such as pencils, rulers, and compasses. The layout engineer would use these tools to draw the circuit on a sheet of paper or a Mylar film [BOPET](Biaxially-orientedapolyethylenexterephthalate) .   
This process was a time-consuming and labor-intensive process that required a high level of skill and expertise. The layout engineer would need to visualize the circuit in three dimensions and create a layout that met the performance, reliability, and manufacturability requirements. As computer-aided design (CAD) technology advanced, the process of layout design began to be done using software. The first EDA layout tools were simple software programs that allowed designers to draw the schematic and layout of their circuits manually. However, these tools were limited in their functionality and were not very efficient.  
Today, EDA layout tools have advanced significantly, and they are the primary means of layout design in the electronics industry. These tools use a combination of algorithms, heuristics, and user input to optimize the placement and routing of components on a circuit board, while taking into account factors such as signal integrity, thermal management, and manufacturing constraints. EDA layout tools have many advantages over manual layout. They are much faster and more efficient, and they can handle the increasing complexity of modern electronics design. They also provide a high level of accuracy and consistency, which is critical for ensuring the performance and reliability of the circuit. Overall, the evolution of layout design from manual layout in the past to the EDA tools that are used today has been driven by advances in computer hardware and software, as well as the increasing complexity of integrated circuits.

**The Problem of Analog Layout Design**

This section describes some aspects of analog layout design that are important for understanding the work presented here and introduces technical terms that will be covered in the rest of this thesis . As mentioned in Section 1.1, the problem of analog layout design is to take a given electronic circuit and turn it into a physical representation, which is itself also called a layout design. The purpose of that physical representation is to describe the detailed chip geometries on the photolithographically masks which need to be created for the various layers of the semiconductor manufacturing process . These geometries include the layout of the circuit components and their electrical interconnections with interconnect holes between isolating layers, as well as the so-called bond pads for the chip’s connections to its periphery, Converting an electronic circuit into a practical layout requires consideration of many design restrictions and design objectives that arise from understanding the circuits function. Thus, the readability of a schematic diagram is not only for circuit designers but also for layout designers.

* + 1. **Design Restrictions and Design Objectives**

From a mathematical point of view, layout design is an optimization problem and can be regarded as a search for an optimal solution inside a huge solution space. Thereat, design restrictions define a valid region in the solution space, while the design objectives specify an optimum inside that valid region, as depicted in [[[2]](#footnote-2)]. Design restrictions are commonly divided into three categories:

* **Technological restrictions :** are meant to ensure the manufacturability of the (IC) . They are derived from the chosen semiconductor technology and formulated as geometrical design rules. Design Rule Check (DRC) can be very complex, but most of them belong to one of the following groups: minimum width, minimum distance, minimum overlap, or minimum enclosure.
* **Functional restrictions** (electrical restrictions) are supposed to guarantee the circuit’s proper electrical functioning. They can be separated into circuit-specific requirements (e.g.,to prevent unwanted coupling effects) and process-specific requirements (such as the limitation of current density in electrical wires to avoid electromigration).
* **Design-methodical restrictions** are deliberately introduced to reduce the complexity of the layout design problem, thereby making the design task amenable to computer-aided automation approaches. An example is given by layer-dependent wire directions for the purpose of automated routing (e.g., metal1: horizontal, metal2: vertical).

**Process Design Kit (PDK) and Design rules[[[3]](#footnote-3)]**

A **PDK** is a collection of files, libraries, and design rules that provide the information and tools necessary for designing ICs using a specific fabrication process. The PDK includes a range of design rule checks (DRCs) and layout versus schematic (LVS) checks to ensure that the layout of the IC meets the requirements of the fabrication process. The PDK also includes models for device simulation and characterization, allowing designers to simulate the behavior of the IC under different operating conditions.

**In our work we** use Saed\_pdk\_32\_28 is a Process Design Kit (PDK) developed by the Semiconductor Advanced Electronics Design **(SAED**) group at Ain Shams University in Egypt. it appears that the design rules for Saed\_pdk\_32\_28 are based on micron (µm) measurements, rather than lambda-based rules. Lambda-based rules are typically used in deep submicron processes, where the feature sizes are smaller than the wavelength of light used in photolithography. The 0.35 µm technology node is not considered a deep submicron process,

* 1. **Levels of Design Hierarchy**Analog IC layouts are usually built in a hierarchical fashion, which is achieved by putting design components inside other design components. Basic design units such as transistors are usually provided as primitive devices i.e. basic cells with no sub-hierarchies. At a higher level a group of design elements that together form a functional unit can be contained in a single (but in a hierarchical case) cell. Functional units become modular library components that can be instantiated in layouts like base units. To avoid semantic confusion when talking about units it is best to classify them according to these characteristics based on their position in the design hierarchy , For that purpose, this thesis proposes and adheres to the following terminology

|  |  |  |  |
| --- | --- | --- | --- |
|  | Hierarchy Level | Examples | Degree of  (Re-)Utilization |
| Blocks | Block Level | Variable Gain Amplifiers (VGA) | Low |
| Advanced Modules | Module Level | Operational Transconductance Amplifiers (OTA), Differential Amplifiers, | Medium |
| Simple Module | Module Level | Differential Pairs, Current Mirrors, | High |
| Primitive Device | Devices Level | Transistors, Resistors, Capacitors , Guard rings | Very high |

table 1.1: Classification of hierarchical cells in analog/mixed-signal design

* 1. **Main Design Tasks:  
      Device Generation, Floorplanning, Placement, Routing**

|  |  |  |  |
| --- | --- | --- | --- |
|  | Floorplanning | Placement | Routing |
| Considered Components | Circuit Blocks (treated as black boxes) | Primitive Devices and Modules | Wire Segments + Vias (to cross metal layers) |
| Quantities to be set by the Design Task | * Block Locations * Aspect Ratios * Pin Positions | * Locations * Orientations * Layout Variants | Wire Paths, Segment Layers and Widths + Via Positions and Sizes |
| Typical Restrictions | * Rect. Chip Outline * Block Distances * Chip Regions | * Block Outline * Space for Routing * Parasitics | * No Wires Above Devices * Available Metal Layers * Parasitics and Currents |
| Primary Objectives | * Minimize Area and Wirelength * Optimize Power Supply and Current Flow | Device Matching | Minimize Number of Vias and Number of Metal Layers |

Table 1.2 The main tasks in analog layout design

* + 1. **Device Generation** in layout refers to n is the task of creating the layouts for the individual components of the given input circuit. Here for, every component needs to be individually layouted according to its respective sizing (e.g., the channel width and channel length of a MOS transistor). In the past, this task has been an integral duty on the shoulders of an IC design team. Today it is common practice that the primitive devices of a semiconductor technology are readily delivered by the vendor as part of a so-called process design kit (PDK), which is  involves creating the metal interconnects, transistors, and other components that make up the circuit, and optimizing their placement, spacing, and routing to meet the requirements of the technology node. It is an iterative process that involves simulation, testing, and optimization. Designers use simulation tools to model the performance of the circuit and identify potential layout issues, such as parasitics or timing violations. They then make adjustments to the layout, such as changing the placement of components or adjusting the width of metal interconnects, and test the circuit again to verify that the changes have improved its performance. Device generation in layout is a critical step in the design of integrated circuits, as it determines the physical structure of the circuit and its performance characteristics. Even primitive devices have an immense layout variability, and one major source of this variability is device folding. For example, a MOS transistor can be folded by changing its so-called number of fingers. As shown in Figure 1.2, the transistor variants thus have different aspect ratios while preserving the total channel width and channel length. Device generation is already important during floorplanning for estimating the total size of a layout block.

**total width = width per finger \* num of finger\*num of multiplier**

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تم إنشاء الوصف تلقائياً

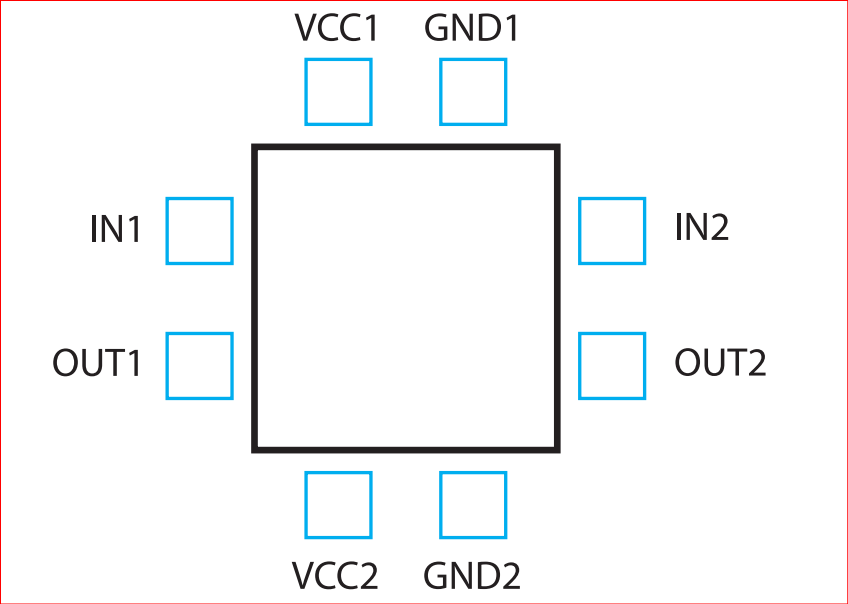
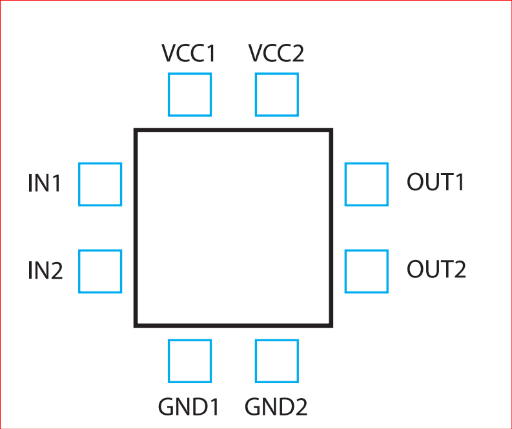
figure 1.2 : Different layout variants of a MOS transistor with the same total channel width and length.

**Fingers and multipliers**

* + 1. **Floorplanning** is the task of specifying locations, aspect ratios, and pin positions for the layout blocks of a chip. Therein, each block is treated as a black box whose area is roughly estimated by the floorplan designer from generating the block’s devices. For economical and electrical reasons, the primary objectives in floorplanning are to minimize the total layout area and the total wirelength, as well as to optimize the power supply and the current flow. A hard restriction concerning the layout area can be that the blocks must fit into a fixed outline, depending on the semiconductor package chosen for the physical sealing of the chip during the final stage of the fabrication. In general, the top-level chip boundary is demanded to be a rectangle whose aspect ratio should not depart too far from a square. In the context of wirelength minimization, some blocks are required to be positioned close to the chip boundary because they will later be connected with the periphery. On the other hand, it may also be necessary to keep a certain minimal distance between dedicated blocks such that sensitive signals are not disturbed by unwanted thermal and electrical influences. A large block can contain subordinate blocks that also need to be floorplanned

**Pin-Driven Planning:** The pin-out is the first step of your floorplan in which you may participate as a mask designer. Some refer to it as the pad-out. This is the process in which the input and output pins that will surround the chip in its packaging are defined.

The pin-out directly affects your work. The quality of your pin-out directly affects how good your chip floorplan will be and how easy the chip will be to layout  
**You could use the same package and the same signals, but use the various signals to be in very different places. Very different pins placement will produce a very different layout as same as in the next figures.**



**To Obtain A good floorplanning [8] :**

• Start thinking about the layout when doing the schematics. Think about how this schematic translates to the layout.

•Industrial quality layout.

• Compact rectangular layout.

• Input and output on the two sides.

•VDD and VSS on the top and bottom.

• N-well all around

• User-defined connectivity requirements for every layer, in addition to net-based routing constraints, handle the results of analogue signal crosstalk, minimum capacitance, and resistance.

• Understands the various divisions or blocks of a design.

• Understands the important features of each block: size, aspect ratio, and pins.

• Dynamically displays the connectivity between blocks and connections to the pads.

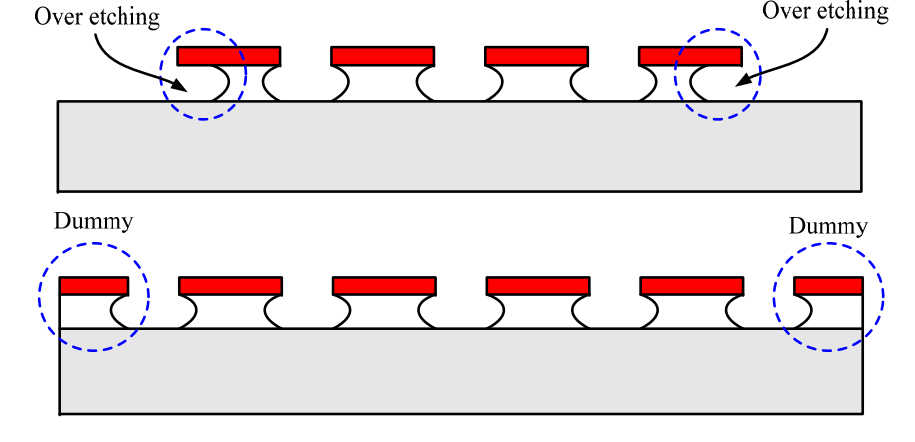
• Allocates space for routing based on the number of routing layers.

• Places each block and optimizes the pin locations for each block based on the overall connectivity requirements and the feasibility of routing the signals between blocks.

• Places top-level ports based on constraints.

floorplan made the electron’s life travels from one side to the other easier.

•Use dummy elements to improve symmetry and avoid Gate Etching Effect.



• Matched transistors are used extensively in both analog and digital CMOS circuits.

• Keep sufficient spacing between power blocks and sensitive blocks.

• Use Guard rings for isolation and guard Ring is a useful tool to protect our circuits from parasitic effects and so that chances of latch-up are reduced.

**Neat fly lines indicate good floor planning [8] :**

* **Bad**

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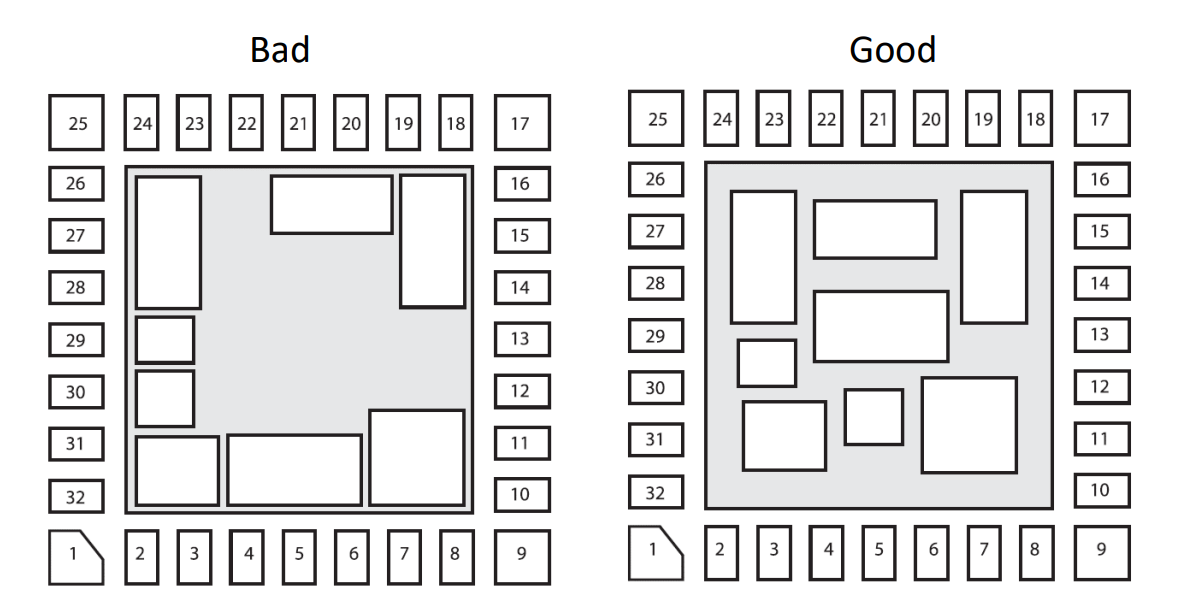
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* **Good**

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تم إنشاء الوصف تلقائياً

* Minimize The area as possible is Perfect but be care to leave a good space for routing and decoupling caps .



* Inputs and outputs should be placed near the correct cell blocks.
  + 1. **Placement :** it is not only means to move the layout components into appropriate locations, but may also require to rotate them and to vary their layout without affecting their electrical function (for example by changing the number of fingers discussed above), such that all components fit into the block outline defined during the floorplanning phase. As in floorplanning, it is desired to obtain a device placement wherein the total area and wirelength are minimized, but usually these objectives first and foremost stem from the need to obtain a good device matching. The same is true for higher-level modules whose placement aims at achieving an overall symmetry of the layout block where the modules are placed in. Opposing the need to place the components close to each other, a common demand is that a sufficient amount of space must be reserved between the components to accommodate their routing.
    2. **Routing :** refers to the process of creating the physical connections between the various components of an electronic circuit. This involves designing the metal interconnects that link the transistors, resistors, capacitors, and other components of the circuit, and optimizing their placement and routing to meet the specific requirements of the design. Routing in layout is a critical step in the design of electronic circuits, as it determines the physical structure of the circuit and its performance characteristics. The routing process involves creating the metal tracks that connect the different components of the circuit, and optimizing their placement and routing to minimize parasitic effects such as resistance, capacitance, and inductance.

The demand to allow for routing space between layout components is rooted in the fact that sensitive circuitry often forbids electrical wires to be drawn above these components. this has to be taken into account during the routing task. Another restriction is to confine which metal layers are available for the routing. On the lower design levels, a common agreement is that only the first two (M2 , M3 ) of the available metal layers may be used in order to retain the remaining metal layers for the later top-level routing. Leading a wire across different metal layers requires to connect the respective wire segments with a VIA (vertical interconnect access). The size of a via and the width of a wire segment must be set with respect to the expected current load.

**Primary objectives in routing are :**

* to minimize the number of vias (i.e., to avoid crossing between metal layers if possible),
* to minimize the number of metal layers (and thus the number of necessary photolithographically masks),

**Some important Rules which should follow in Routing:**

* Choose routing layers based on process parameters and circuit requirements. For each process a standardized list of routing layers should be determined based on layer resistance and capacitance. Layers such as N-well, active, and high-resistance poly gate are not used for routing.
* Priorities between routing layers can also be standardized using the same criteria [8].
* Use of more number of columns and rows vias.
* The use of metals with an odd number for vertical wires and an even number for horizontal wires to avoid interference between metals and each other.
* Minimize total run time for carrying out routing process [8].
* Minimize total wire length.
* Avoid too much parallel routing of metals (to decrease parasitic capacitance [8].
* Increase the width of the wire to overcome Electro migration [9].

**صورة تحتوي على لقطة شاشة, مستطيل, ميدان/ مربع, نص

تم إنشاء الوصف تلقائياًManhattan routing rule**:  also known as the Manhattan style or Manhattan distance, is a common technique used in analog layout design to route interconnects between components. It is named after the street layout of Manhattan, which is characterized by a grid of perpendicular streets. The Manhattan routing rule involves routing interconnects in a series of right-angled, orthogonal segments, either horizontally or vertically. This ensures that the interconnects are parallel to the edges of the layout grid and minimizes parasitics such as capacitance and inductance. Using it also to reduce the common area between metal layers. For example, if Metal 1 is routed in horizontal direction. Is required to route M2 in vertical direction as shown in Figure (1.3)

Figure 1. 3 Manhattan routing rule

While design restrictions are strict confinements which must definitely be satisfied, design objectives represent gradual optimization goals that are pursued as good as possible. They can be roughly classified into economic optimization goals and functional optimization goals. Economic optimization goals include the reduction of product costs (e.g., by minimizing the total chip area and the number of required metallization layers) as well as reducing the development costs (e.g., by minimizing the design effort via design automation). Examples for functional optimization goals are the minimization of the total wirelength as well as optimizing the chip’s heat dissipation to prevent critical hot spots. One of the key advantages of the Manhattan routing rule is that it is easily automated using computer-aided design (CAD) tools. This allows designers to quickly and efficiently route interconnects in complex circuits, saving time and reducing errors. However, the Manhattan routing rule also has some limitations. For example, it may not be the most efficient routing strategy for certain types of circuits, such as those with high-frequency signals or those with non-orthogonal components .[[[4]](#footnote-4)]

As the name implies, functional restrictions and functional optimization goals pertain to the functionality of an integrated circuit. Herein, three basic issues can be embraced by the term functionality:  
• Does the circuit work accurately enough to perform the desired function?  
• How well is the circuit set up against long-term failure owing to effects of degradation?  
• What measures are taken to prevent an instantaneous malfunctioning due to fabrication problems?   
The answer of those issues will be postponed to chapter 3

**Chapter 2**

**Learning phase and literature Review**

**2.1 Learning phase**

We started by learning the basics of VLSI, moving on fabrication process and devices fabrication, fabrication problems and analog layout issues. We’ll talk about this learning phase by two sections:

• Illustration these basics before starting on the main topic to be on common ground.  
 • Discussing the Layout or the standard cells we have done in the learning phase.

**2.1.1 VLSI (Very Large Scale Integration) overview**

1. **Design**: VLSI design involves the creation of a circuit specification, logic design, physical design, and verification of the circuit's functionality.
2. **Fabrication**: Once the design is complete, it is transferred to a semiconductor fabrication house.
3. **Testing**: After fabrication, the IC is tested to ensure it meets the design specifications and works as intended.
4. **Technology nodes**: VLSI technology is classified based on the size of the transistors and other components on the chip. The smaller the components, the more advanced the technology node is considered.
5. **Moore's Law**: This is a prediction made by Gordon Moore, co-founder of Intel, that the number of transistors on a chip would double every 18-24 months, leading to increased performance and reduced cost.[ **[[5]](#footnote-5)]**
6. **Applications**: VLSI technology is used in a wide range of applications, including microprocessors, memory chips, digital signal processors, and application-specific integrated circuits (ASICs).
7. **CAD tools**: Computer-aided design (CAD) tools are used extensively in VLSI design to automate the design process and reduce errors.
8. **Challenges**: As the number of transistors on a chip increases, several challenges arise, including power consumption, heat dissipation, interconnect delay, and manufacturing yield.
9. **Design styles**: There are two primary design styles in VLSI: full-custom and semi-custom design. Full-custom design involves designing every component of the chip from scratch, while semi-custom design involves using pre-designed components and interconnecting them to create a new design.
10. **Future of VLSI**: The future of VLSI is expected to involve the continued scaling of technology nodes, the development of new materials and manufacturing techniques, and the integration of new technologies such as artificial intelligence and quantum computing into IC design.

**2.1.2 IC Fabrication process**The fabrication process creates the physical components of the circuit, such as transistors and resistors, while the layout design determines how these components are arranged and connected to create the desired circuit functionality. The two processes are interdependent and must be considered together to create a working and reliable integrated circuit.

**Basic steps of IC fabrication**:

• Wafer production • Epitaxial growth   
• Photolithography • Masking   
• Etching • Doping   
• Atomic diffusion • Ion implantation   
• Metallization • Assembly and packaging

**Chapter 3**

**Challenges and Solutions in Analog Layout Design**

Analog layout design is a critical step in the development of analog circuits, as it involves creating a physical representation of the circuit that can be fabricated and tested. However, this process can be complex and challenging, as a range of factors can impact the performance of the circuit. In this chapter, we will explore some of the common challenges that can arise in analog layout design, including matching and symmetry, parasitics , crosstalk and electromigration. We will also discuss strategies and techniques for addressing these challenges, including layout By understanding these challenges and approaches to addressing them, designers can create analog layouts that meet the required performance specifications and are manufacturable.

**3.1 Matching[[[6]](#footnote-6)]**

In short terms, matching is employed to obtain analog signal accuracy via “electrical symmetry”. This can be understood as follows. The manufacturing tolerances exhibited by the many steps of an IC fabrication process are so large that their cumulative effect causes an unbearably high deviation in a component’s parameters from their desired values . Hence, Analog circuits often use structures like differential pairs and current mirrors, where the matching of device characteristics such as the threshold voltage Vt is important. Circuits using these structures with device threshold differences of a few millivolts or less can determine the performance and yield of a design. The threshold difference between a pair of (otherwise identical) MOS devices is due to the variations in number of doping atoms in the channel. Matching is an important consideration in the design of analog circuits, particularly those that require precise matching of components, such as transistors and resistors, to achieve optimal performance. Matching can be a challenge in layout design, as process variations and layout constraints can impact the matching of components. One common challenge in matching is achieving symmetry between components. For example, in a differential amplifier, the two halves of the circuit must be matched in terms of component values and placement in order to achieve balanced operation. This can be challenging in layout design, particularly when layout constraints limit the available space for components. Another challenge in matching is achieving matching across different parts of the chip. For example, in an op-amp design, the input and output stages must be matched in terms of component values and placement in order to achieve optimal performance. This can be challenging when the input and output stages are located on different parts of the chip.  
However, matching also requires careful layout techniques to minimize the differences in device parameters due to distance, lithography variations, rotation, process variations, biasing, and temperature gradients on the chip.

Mismatching in (IC) integrated circuits is generally of two types:

* **Random mismatches:** the error resulting from that one can’t be identified or controlled while implementing the layout, it will happen during the fabrication and the reasons behind that are the non-uniform etch rate, the doping and finally the wafer itself. errors by variations in the thickness of oxide layers, variations in the doping level of transistors, and variations in the width and length of metal interconnects. These variations can lead to differences in the performance of individual components, even when the components are designed to be identical
* .**Systematic mismatches :** which is due to non-uniform thermal distribution during fabrication process, it can be solved by proper layout techniques, best device matching so as to be as close as possible to the needed performance. Systematic mismatches are caused by: Process biases, Mechanical stress, Temperature gradients, and Polysilicon etch rates, etc

Process variation during fabrication process limits accuracy and desired performance of analog circuit:

* + Mask production and alignment: Masks may not be 100% perfectly aligned over the wafer, resulting in changes in device properties.
  + During fabrication process variations limits desired performance of analog circuits. Process variation examples: Lateral diffusion: There is no control over diffusion profiles in the substrate. Diffusion materials can diffuse to great distances under source and drain regions causing differences between matched device groups. Solution: Increase distance and use dummy structures that affect all transistors the same.
  + **over etching**: : Etchants with various types; wet, dry, anisotropic or isotropic can cause over etching in certain areas, hence producing a mismatch in the devices. Poly silicon does not always etch uniformly.

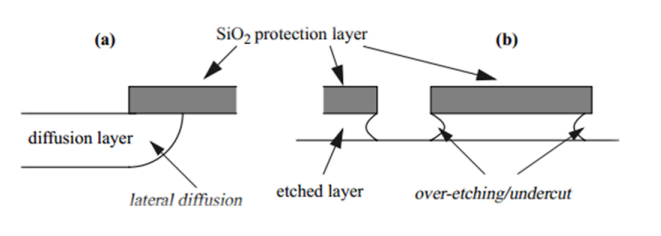


figure 3.1 Etching effects

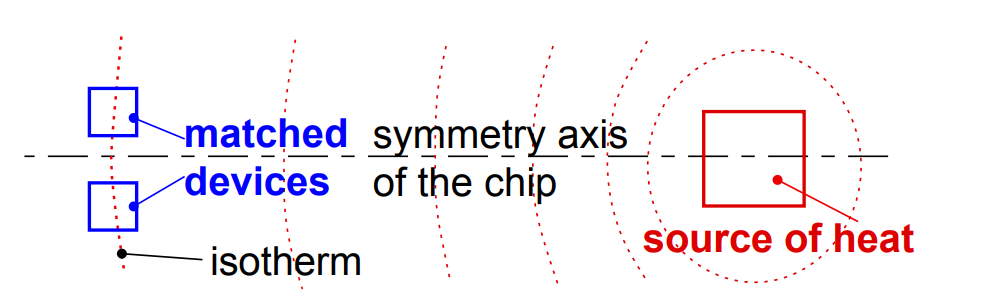
* + Large openings etch faster than small openings in mask. Solution: is to use dummy structures.

And all of this effects on Dimensions of device Ratio and consequently the threshold voltage value will change with it.

صورة تحتوي على الخط, خط, ساعة حائط, لقطة شاشة

تم إنشاء الوصف تلقائياً

* + - Mismatch (Placement and Gradiant)
    - Orientation
    - Stress gradient: occurs mainly from wafer dicing where stress is highest at edge of the chip, Packaging can cause stress in chip. Solution: Keep critical matched devices in center of chip , Avoid using corners for matched devices
    - Temperature gradient We use matching so that the devices are exposed to the same thermal effect



The devices have the same orientation, are close to each other, and are interleaved as neighbors to each other. We have satisfied the three main rules, When these components are etched, the ones in the middle of the block see very different conditions during processing than the ones on the ends. The resistors on the ends might etch more, making them slightly narrower than the ones in the middle

Figure 3.2 Edges of blocks etch differently than middles of blocks.

To reduce the impact of process variations and parasitics (will be illustrated) and improve performance we use dummy components.

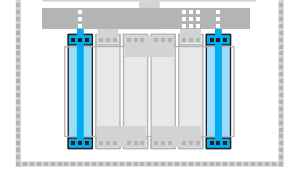
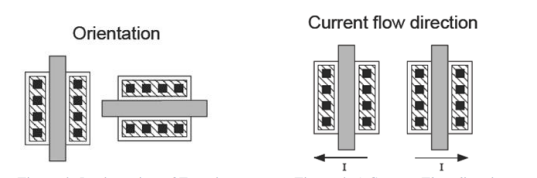
**Dummy components**, also known as "fillers," are non-functional components that are added to the layout of an integrated circuit to improve performance and reduce the impact of process variations and parasitics. They are typically made of the same materials as the functional components and are designed to match the physical characteristics of the functional components. There are several types of dummy components that can be used in layout design, including dummy resistors, dummy capacitors, dummy transistors, These components are strategically placed in the layout to achieve specific goals, such as matching the resistance . Dummy resistors are often used in analog layout design to match the resistance of functional resistors and reduce the impact of process variations. They are typically placed in parallel with the functional resistors and have the same dimensions and materials as the functional resistors. Dummy transistors are non-functional transistor structures that are added to the layout to match the parasitic capacitance and resistance of functional transistors and reduce the impact of process variations. They are typically placed in parallel with the functional transistors and have the same dimensions and materials as the functional transistors. designers can identify the optimal placement and number of dummy components to achieve optimal performance . Notice we shorted the dummy resistors together and tied them to ground or (VDD). They are not part of the circuit. They are only there to give the outer two circuit resistors similar conditions for etching as the inner two circuit resistors  
dummies are used to balance the effects on the lateral transistors, they may be used as well to shield all around the devices in smaller and more sensitive technologies

Figure 4 2Two dummies to help the four circuit resistors etch

Before talking about matching techniques let’s see the Rules for MOS transistor matching:

**Rules for optimum matching:**

**Devices to be matched should have:**

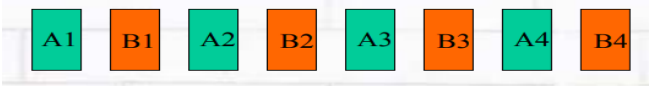
1. Same structure
2. Same temperature
3. Same shape and same size
4. Minimum distance
5. Common centroid geometries
6. Non-minimum size
7. in the areas of low-stress gradients.
8. in close proximity.
9. Critical devices need to be placed in the same Poly orientation to have the same current flow and reduce any mismatch resulting from different orientations. Same surroundings (same neighborhood)
10. the layout as compact as possible
11. Place transistors well away from the power devices.
12. For current matching keep overdrive voltage large.
13. For voltage, matching keeps overdrive voltage smaller
14. Whenever possible use Common centroid layouts as will be illustrated.

To address these challenges, layout designers may use a range of techniques and strategies[[[7]](#footnote-7)]. For example:

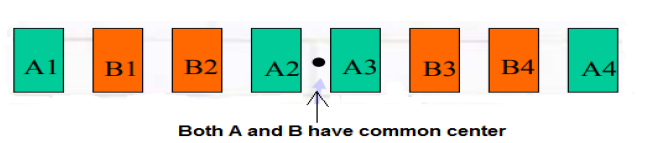
* **common centroid** layouts can be used to achieve component symmetry, by placing components in a symmetric pattern around a central point.
* **inter-digitiation** : In an interdigitated pattern, all the transistors are in an interleaved pattern like suppose there are two transistors A & B with 2 fingers each. then ABAB or ABBA or AABB called interdigitation

Let's say we have two devices A,B )A and B can be anything likes transistor, resistor, and capacitor) and split A and B into 4 small multipler A1-A4 and B1-B4.

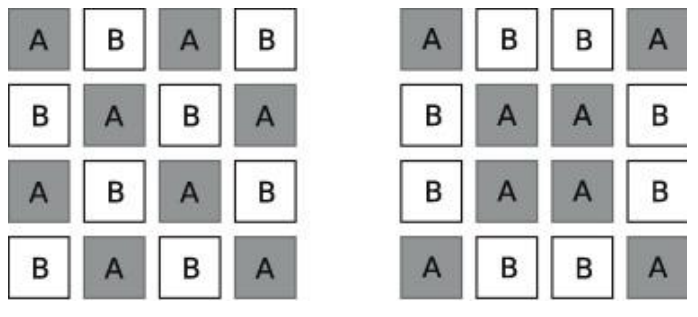
**Inter-digitization technique**: Placing alternate components and Process gradient almost evenly distributed between components A and B. , and Placing Alternate components , this technique is mainly used in differential pair to reduce noise and interference by increasing the coupling between the two traces. This achieved by altering the placement of the two traces such that they interdigitate with each other , this interdigitate pattern causes the electric fields generated by the signals in each trace to overlap more closely, increasing the coupling and canceling out even more noise . interdigitization can also reduce crosstalk ( will be illustrated)



**Common centroid technique**: all components have same centroid , The devices should be symmetrical, and Their orientation should be the same  
Common centroid technique is mainly used in current mirrors, since it mainly focuses on having all devices aligned at a common centroidal point with respect to the main diode connected device.



Example of the two way



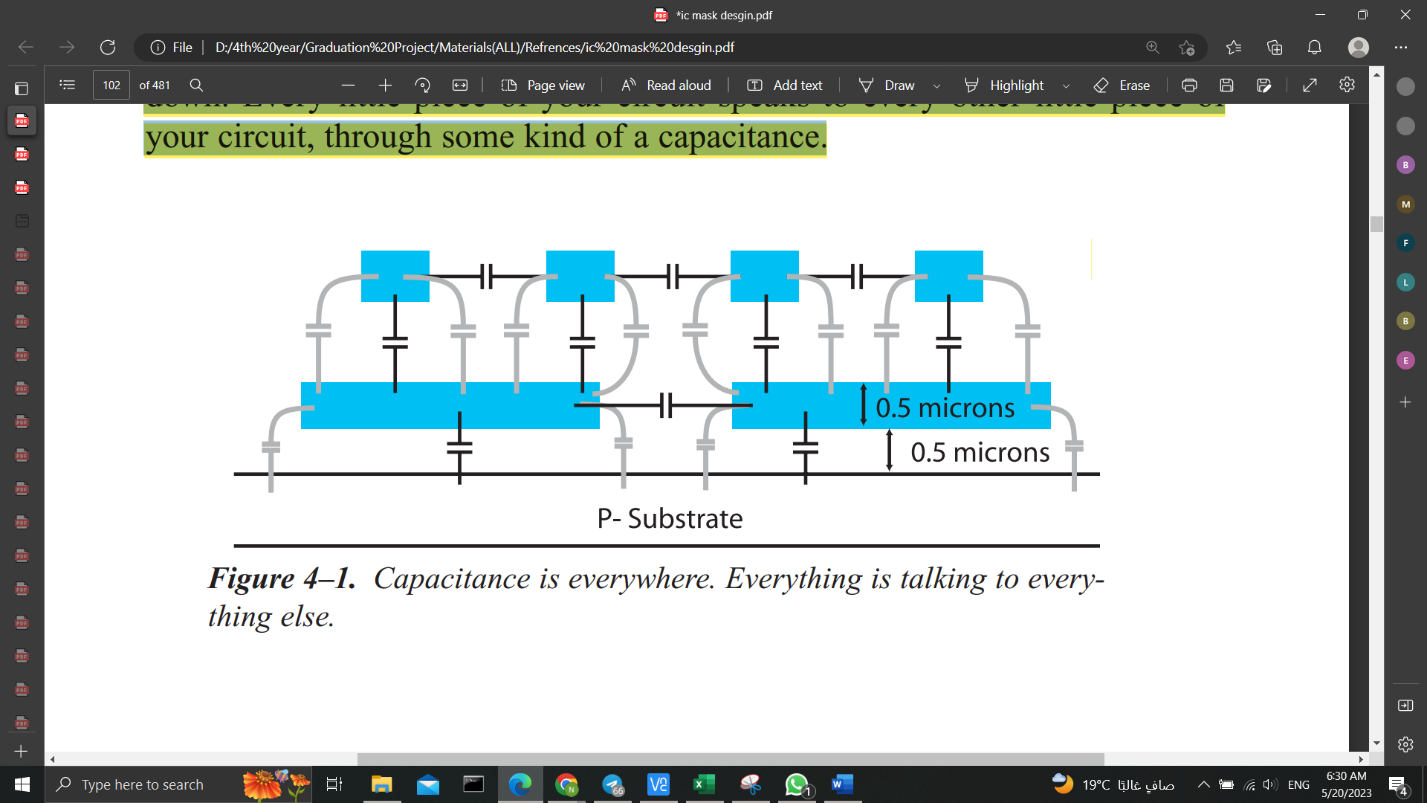
Inter-digitation common centroid

**3.2 Parasitics**

Parasitics are a common challenge in the design of analog and mixed-signal integrated circuits. They refer to unwanted capacitance, inductance, and resistance that are inherent in the physical structure of the circuit and can have a significant impact on its performance. These parasitics can impact the performance of the circuit in a variety of ways, such as reducing its speed, increasing its power consumption, or degrading its noise performance. in analog and mixed-signal circuits, the impact of parasitics is particularly significant, as these circuits often require precise matching between components and are sensitive to changes in their physical environment. For example, parasitics can cause imbalances in differential amplifiers, reduce the gain of operational amplifiers

1. **Parasitic capacitance [[[8]](#footnote-8)]  
   Where do parasitics come from?**

You can find them everywhere, really. As we said earlier, every time you run a wire or you run a gate stripe or you create anything in a chip, you get some kind of parasitic.To illustrate how prevalent parasitics can be, let’s look at four metal traces above two other metal traces small blue boxes In Figure (3.3) . Between each of these wires, there is effectively a parallel plate capacitor. There is also a capacitance from each of the four wires down to the lower layer, and from the lower layer to the substrate. We also have the fringe capacitances all the way down. Every little piece of your circuit speaks to every other little piece of your circuit, through some kind of a capacitance.



*Figure 3.3* Capacitance is everywhere. Everything is talking to everything else.

But if you have a circuit that is very insensitive to capacitance, let us say like a power regulator, or something else that is quite hefty in the circuit, then you really do not

care about these little extra capacitances all over the place.

However, the faster you go, the higher the frequency, the higher the speed of

the circuit you are trying to work with, the more important these capacitances

become. They do matter.

***Ignoring parasitics can kill your chip.***   
In most circuits, if you do not pay attention to parasitics, then the parasitics can kill your chip. Typically, when you do analog layout, whether it’s CMOS or Bipolar “it is CMOS in the new technology”, if there is any reasonably high frequency involved, maybe 20 megahertz or higher, you will have to worry about parasitics of some sort.

**Techniques to handle the capacitance:**

* Wire Length

When you reduce the length of the wire, then you are reducing the overlap between the wire and substrate, or the wire and something else that happens to be conducting.

Imagine that you are told some areas of wiring need to be low parasitic, then one of the easiest ways to accomplish that is to keep the wire as short as possible, as mentioned above.

* Metal Selection

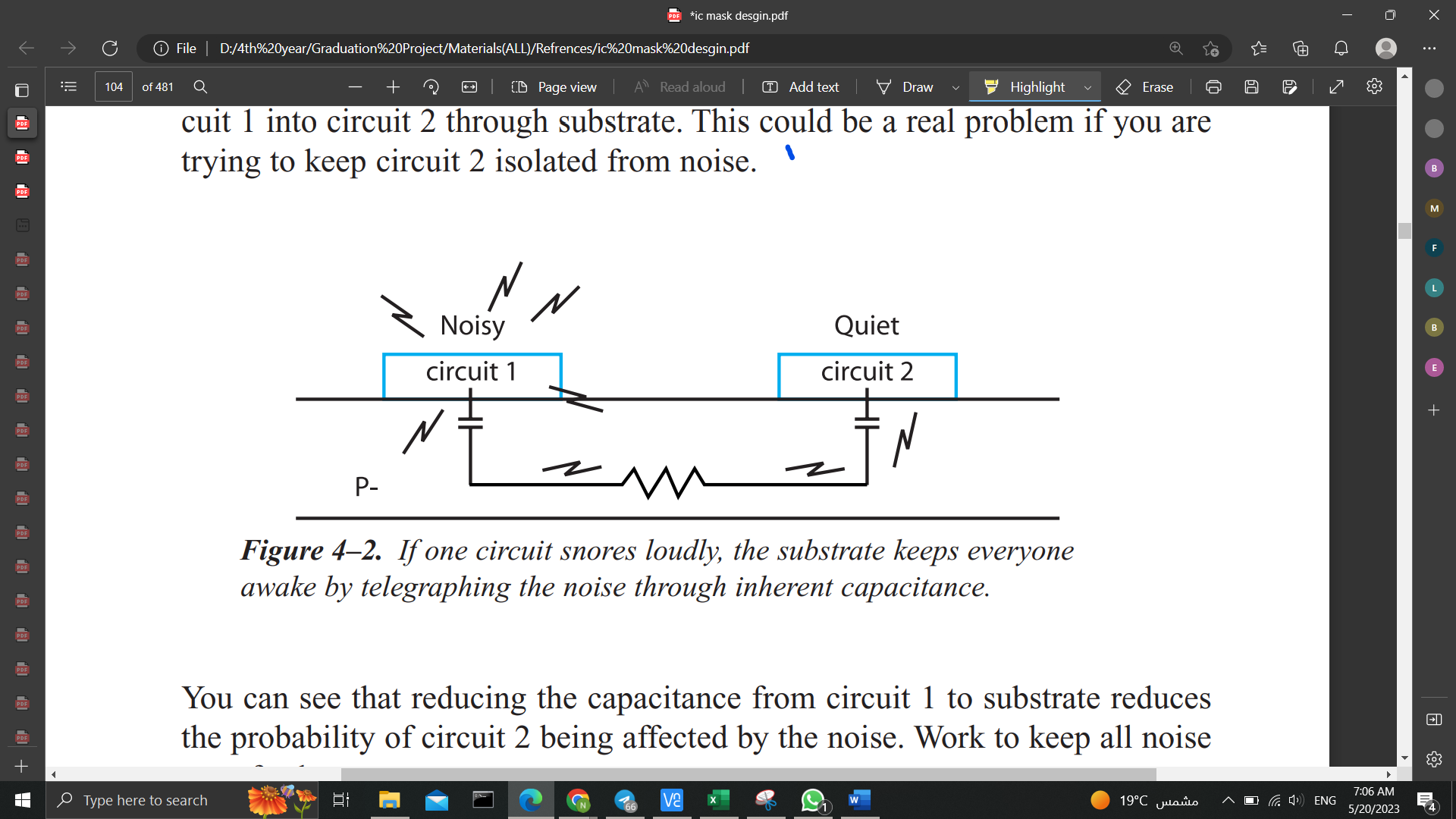
Another solution depends on the metal system that you have available to you. And that is since the type of the metals used in the layout are sometimes is decided by the manufacturer.

The dominant capacitance issue is usually the capacitance of the wire going

down to substrate. That capacitance is the one you are most interested in as substrate goes everywhere. It runs under the entire chip” the black board in the CAD tools is literally a p-substrate”, so any announcement made to substrate is carried to every other component.

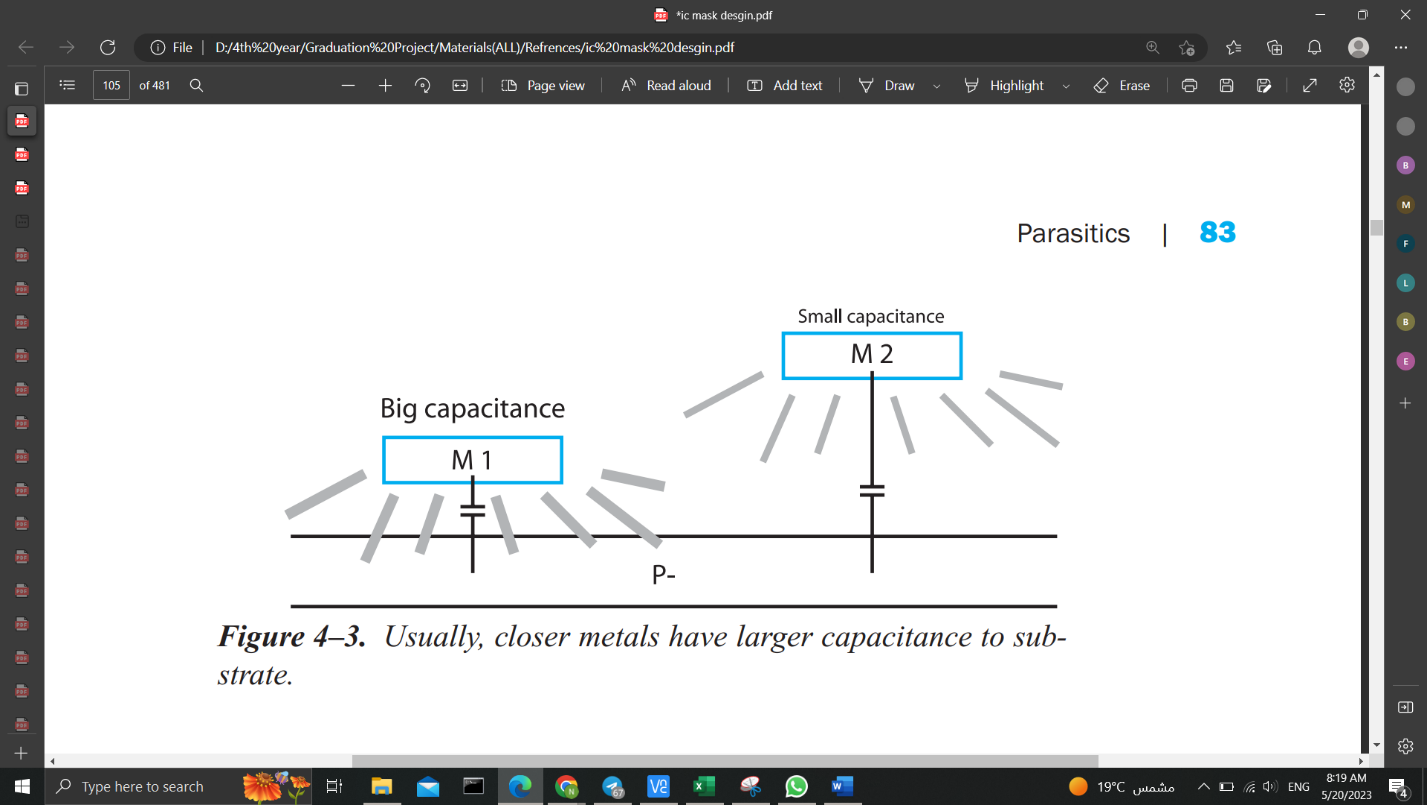
As we can see in figure (3.4) two circuits, each placed in a P-substrate. You can also see that each circuit has a capacitance to substrate. We also have the parasitic

resistance of the substrate itself. The parasitics can couple the noise from circuit 1 into circuit 2 through substrate. This could be a real problem if you are trying to keep circuit 2 isolated from noise.



*Figure 3.4*  If one circuit snores loudly, the substrate keeps everyone awake by telegraphing the noise through inherent capacitance.

Depending on our metal processing, a second way to reduce parasitics is to use the highest-level metal, the metal furthest away from the substrate. Typically, the further we get from substrate the less capacitance we have because the distance between the two plates is a lot further. *Capacitance is inversely proportional to the distance between plates*, like other types of radiation. A little distance makes a lot of difference.



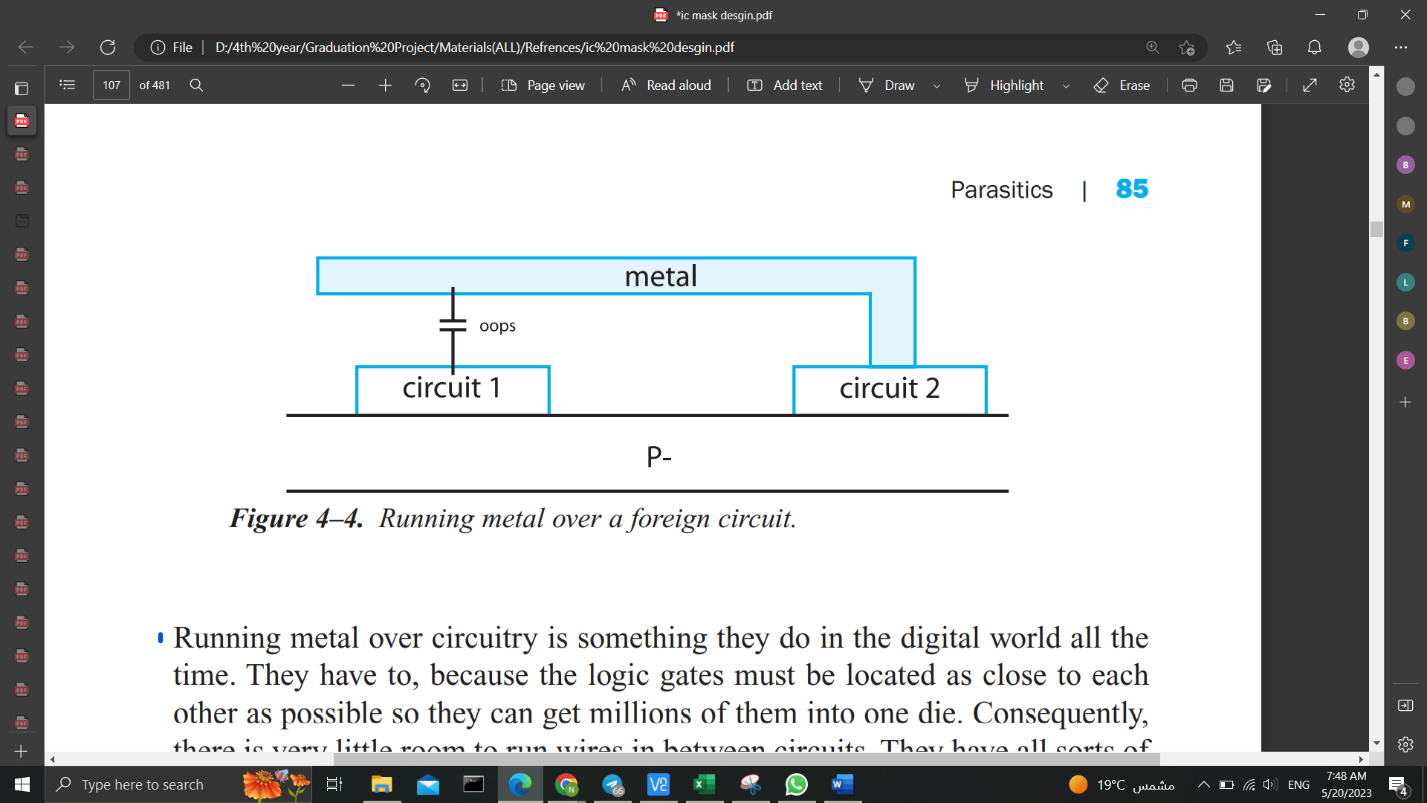
*Figure 3.5*  Usually, closer metals have larger capacitance to substrate

But unfortunately, by just saying that the highest-level metal has the least capacitance is not always true. This is where our particular metal processing could make a difference.

The design rules of the metals may conspire against us. So, we have to look carefully through our process manual to calculate which metal is the lowest capacitance, mainly since the minimum width of these metals may be unique. ***Calculate, don’t assume.***

* Metal over Metal

Up to this point, we have been talking about capacitance to substrate. As we mentioned at the start of the chapter, there are capacitances from everything to everything. For example, consider a circuit with a wire that runs over the top of another circuit. Parasitic capacitance develops between that wire and everything in the underlying circuit.



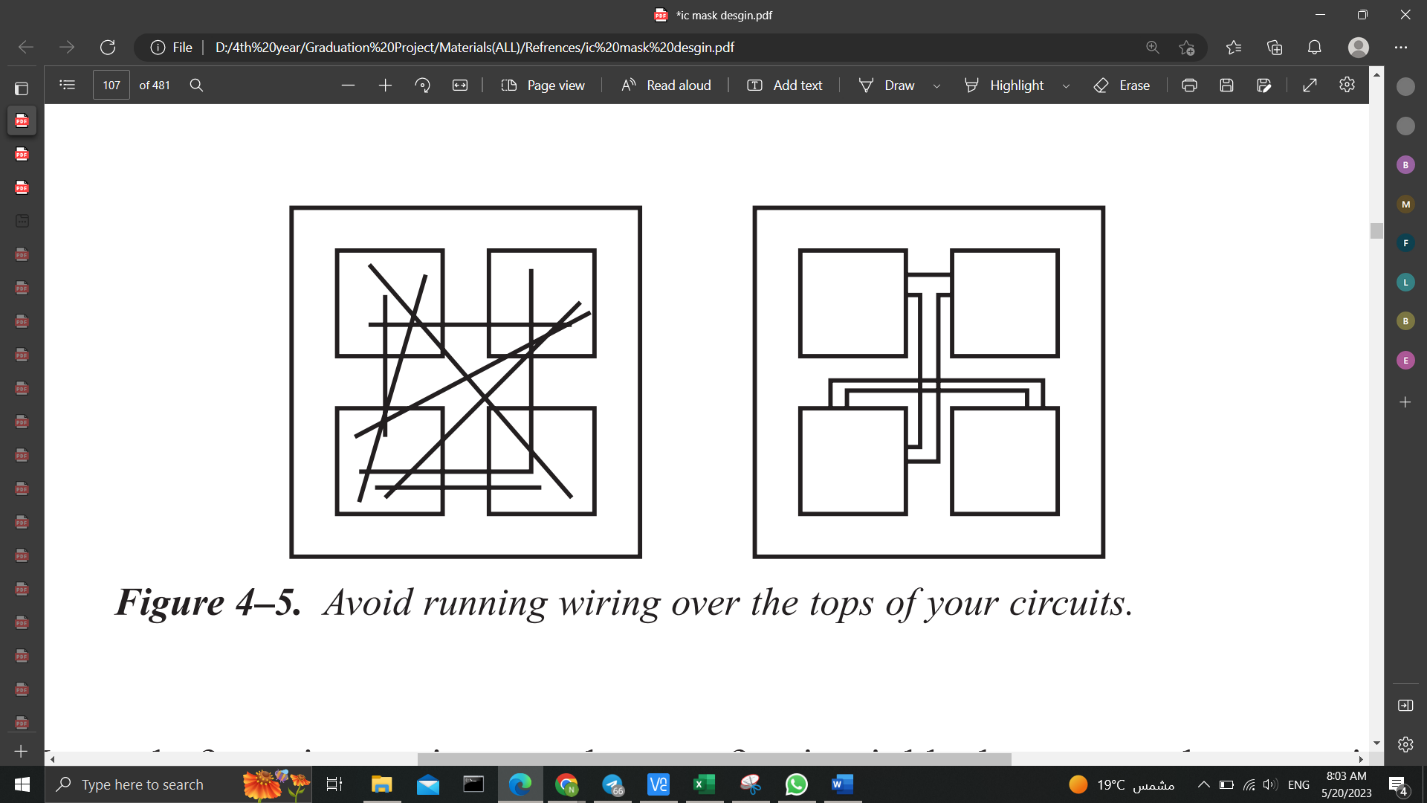
*Figure 3.6* Running metal over a foreign circuit

Running metal over circuitry is something they do in the digital world all the

time. As they have to, because the logic gates must be located as close to each other as possible so they can get millions of them into one die. Consequently, there is very little room to run wires in between circuits. So, they have all sorts of metals running over the top of each other. Then there will be parasitic capacitance to their inverters, NAND gates, flip-flops, and so on.

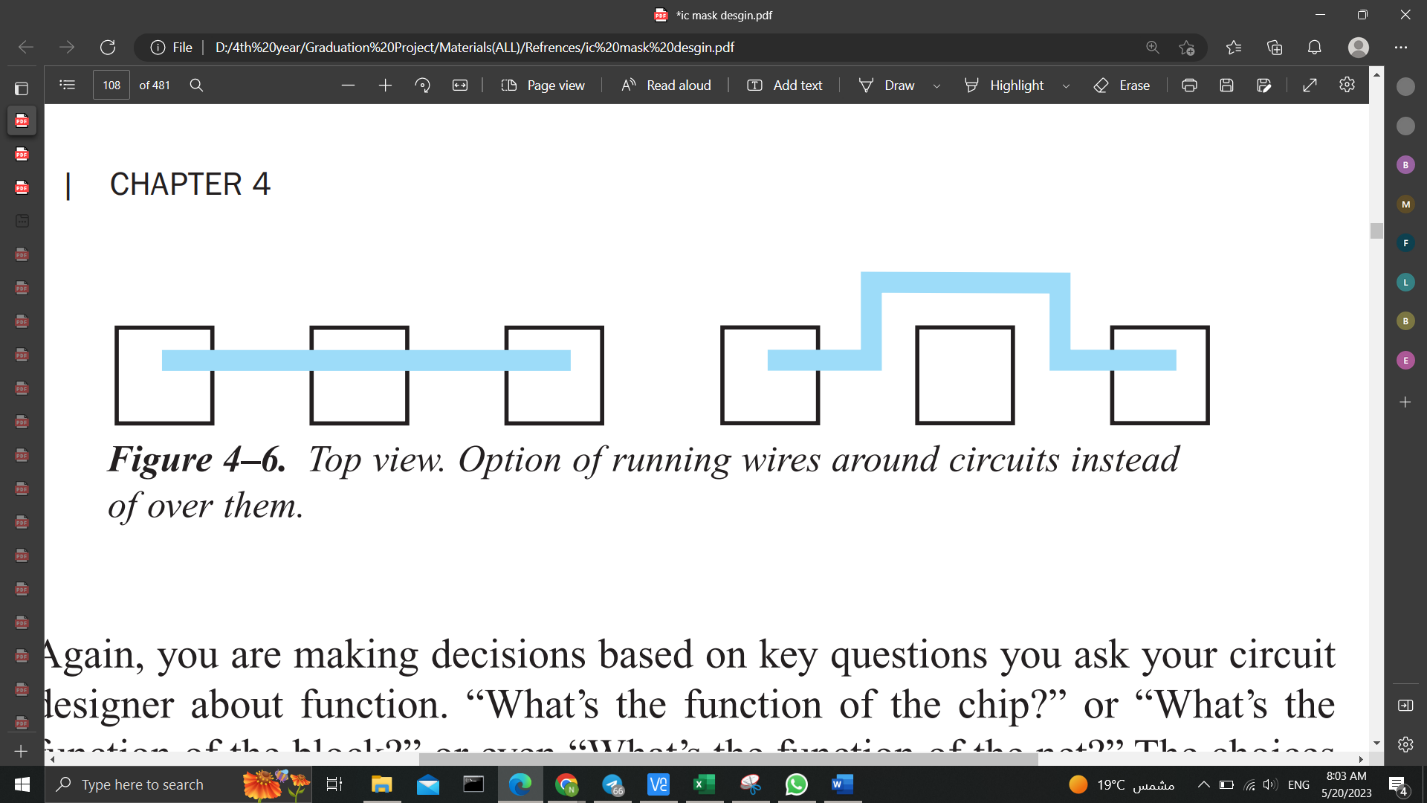
Then assume there can be times when you will have critical wires in a digital circuit that are very sensitive to noise. However, the auto-router says, will put that wire anywhere it well feels like. After all, the auto-router is not paid to think, but just to route. And route it will, regardless of the consequences.

*While with analog circuits*, we typically want to keep sensitive signals away from each other. So, if we had a chip with wires all over the place, it may not work as well as if we had the individual circuits spaced away from each other. With no wiring going over the circuits, just wiring in between the circuits, the parasitics are much more controlled. ***You can kill your chip just by letting the auto-router place your wires without supervision.***



*Figure 3.7* Avoid running wiring over the tops of your circuits

Other way instead of running a wire over the top of a circuit block, is that we may have to wire entirely around a block as it’s a very sensitive node.



*Figure 3.8* Top view. Option of running wires around circuits instead of over them.

Once again, we are making decisions based on key questions you ask your circuit designer about function. such as “What’s the function of the chip?” or “What’s the function of the block?” or even “What’s the function of the net?” The choices you make depend on what the chip is doing. You may just not care about parasitic capacitances with some functions, with others you do.

When we are just designing low-level cell blocks, then the choices are more straightforward. But, when we begin to wire those cell blocks to each other, we have to ask a bunch of questions about an individual wire. which is very different from the digital world where 90% of the wiring is thrown together and who cares about the function.

But we mustn’t forget that, this is an oversimplification, of course, but the point is to let the circuit designer lead you. Ask about all levels of function. After all, you have to know.

1. **Parasitic Resistance**

Another parasitic mentioned at the beginning of this chapter is the *parasitic resistance*. Each wire has a parasitic resistance associated with it. And again, our handling of this parasitic depends on what the circuit does. This time we concentrate on our second question, “How much current does it handle?”.

If we recall, we looked at current densities to see how the amount of current affected our wiring width choice. In addition to wiring width choice, current affects cell-to-cell wiring choices as well.

**Calculating IR Drops**

The power supply in the chip is distributed uniformly through metal layers (Vdd and Vss) across the design. These metal layers have finite amount of resistance. Current begins to flow through the metal layers when voltage is applied to these metal wires, and some voltage is lost as a result of the resistance of the metal wires and current. It is known as an *IR drop*. (Shubham, 2023).

*How the timing is affected*: The Signal Integrity effect known as IR Drop is brought on by wire resistance and current drain from the Power (Vdd) and Ground (Vss) grid. Ohm's law states that V=IR. An unacceptable voltage drop may occur if the wire resistance is too high or the current flowing through the metal layer is greater than expected.

The power supply voltage drops as a result of this unacceptable voltage drop. This indicates that the cells are not receiving the necessary power across the entire design. Due to this, performance suffers and noise susceptibility increases [[9]](#footnote-9)

Let us assume we have a wire that runs from one cell to another cell, which must handle 1 milliamp of current.

We look through our process manual to find the current density capability for this wire. We see that the metal we want to use can handle 0.5 milliamps per micron. That number tells us that we need to make that wire a minimum of 2 microns wide if we expect it to handle 1 milliamp.

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تم إنشاء الوصف تلقائياً*Figure 3.9*  How much will voltage drop as it travels this lengthy wire? Can our circuit handle the drop ?

So, yes, we draw a 2-micron wire. We’re good now! However, what we weren’t told by the circuit designer is that he is worried about the resistance of that wire as well. We calculate the resistance of the wire and let’s say, for example, that the length of our wire from one side to the other is 2 millimeters long. Being 2 microns wide, that equals 1000 squares. (Dividing length by width gives you the number of squares.)

2 mm ÷ 2 µm = 100 squares

Knowing the number of squares in our wire, we go to our process manual to find the resistance of that particular metal in ohms per square. We read that this metal is 50 milli-ohms per square. So, the resistance equals 1000 squares times 0.05 ohms per square.

R = 1000 \* 0.05 = 50 ohms

The resistance through the wire is 50 ohms. Fifty ohms is a significant resistance. That wire is carrying 1 milliamp. Using VIR, you calculate that the voltage drop across that wire is 50 ohms times 1 milliamp. That is a 50-millivolt drop.

V = IR volts

V = 50 \* 1 (ohms)(milliamps)

V = 50 millivolts

The difference in voltage level due to the current in this one piece of wire, is 50 millivolts. If the circuit at the other end of the wire is sensitive to voltage offsets, then we have trouble.

So again, it’s a case of going back to our circuit designer and saying, “we’re just finishing up this chip. I’ve got this really long wire from one side of the chip to the other. You told me it was taking 1 milliamp, so I’m getting a 50-millivolt drop, is that too much?”. But then the circuit designer will say, “that’s huge! That’s enormous! And he is sorry since he forgot to tell you that he needs a maximum of a 10-millivolt drop on that wire or the circuit won’t work properly.” That means we have to make our wire 5 times wider. So, instead of running our 2-micron wire, we apparently need a 10-micron wire. That will lower the drop to only 10 millivolts, which is within the requirements for this particular cell.

these resistance parasitics typically manifest themselves in power wiring because power supply currents are usually pretty big. You can have 20 to 30 milliamps in one power supply. If you have a lot of circuits all connected to the same power supply, it needs to be sized to handle the right amount of current.

**Wiring Options**

We need to know the IR drop limitations and the amount of current flowing in your circuit. When we look at our top-level circuit, we may realize we have to split our power supply wiring into multiple pieces of wire just to handle these conditions. In Figure 3.2.2(b), there is an array of circuits. Their power supply runs along from the bond pad into each circuit as shown. Our circuit designer tells us that the currents for the various blocks are 1 mA, 5 mA, 10 mA, 1 mA, 1 mA, and 1 mA, as noted.

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*Figure 3.10*  Large power drain located furthest from pad creates a problem. (See upper right block)

It appears we have a total of 19 milliamps all coming in from the outside world through the pad on the left. Unfortunately, the block needing the most current is furthest from the pad.

We could size our metal, all the way back to the last block, based on a total current of 19 milliamps. Let’s use our 0.5-milliamp-per-micron example for our wire. In that case, the wire width we need is 38 microns to be reliable. (Total amps divided by amps per micron.)

Just give yourself a big, fat chunk of metal. The whole thing is 38 microns wide.

*Figure 3.11* Option of running thick power wire all along routeصورة تحتوي على نص, لقطة شاشة, برمجيات, عرض

تم إنشاء الوصف تلقائياً

However, we might notice that toward the end of the line we are merely supplying 11 mA. It seems wasteful to use our fat chunky wire at the end. So, what we could do is taper the width as we move along the route.

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تم إنشاء الوصف تلقائياً *Figure 3.12* Stepping down the width as we go saves room

Decreasing the width saves room, just in case we are strapped for real estate. We could start the wire at 38 microns, and then reduce the width as needed.

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تم إنشاء الوصف تلقائياًThere is another option. Why not bring the high current path back to the bond pad independently from the other wiring? You may need to use this option because you can get voltage drops caused by the 10-mA current that affect all the other blocks on the supply. This technique, of course, requires the chip real estate above the array of blocks.

*Figure 3.13* Up and over.

here are all sorts of options. Which method you use depends on the requirements of the circuit, which is based on the circuit function, and on what you’ve been asked to do.

Hopefully you are seeing that knowing a bit about the way the circuit works affects your layout choices. Mask design is not just a case of hooking things up and hoping for the best.

**Rule of Thumb**: If your IR drop is bigger than 10 millivolts, check with your circuit designer.

In order to **reduce parasitic resistance**, make sure that you use the thickest metal. You can usually find the thickness of a metal in the process manual. If the metal thickness is not explicitly stated, then the metal resistance usually is.

***The thickest metal has the lowest ohms per square value.***

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تم إنشاء الوصف تلقائياًIf your metals all have the same thickness, then you can sandwich chunks of metal on top of each other, as in Figure 3.14

*Figure 3.14*Cross-section. Running three metals in parallel to save real estate and reduce series resistance.

In this particular case, you effectively have three metals in parallel. You have reduced the resistance by a factor of 3 for this wire because the current path is shared. In very high current situations, you may do your current density calculations and find, for example, that in order to be reliable, you need a wire 500 microns wide! Running strips in parallel is a good technique to reduce the resistance of high current paths and save yourself some space.

* + 1. **Parasitic Inductance**

When you work with really high frequency circuits, the wires in your circuit start to have a parasitic inductance as well. The way to handle parasitic inductance is to try to model it, so that the inductance is calculated as part of the circuit. Work with your circuit designer right away. Try to develop a floorplan of the chip very early so that the circuit designer can see how long the wires will be. He will incorporate some estimates of the inductances involved.

You may have to choose wires that are much wider than expected. You may have to leave room around certain wires because they are very inductive and very wide. You do not want them to inductively couple into other parts of the circuit.

**3.2.4 Interconnect Parasitics [[[10]](#footnote-10)]**

Having presented parasitic effects *in the bulk*, e.g. Substrate Debiasing, Injection of Minority Carriers (won’t be discussed here), latchup (will be discussed latter ) and *on the surface of silicon,* e.g. Parasitic channel effects, Hot carrier injection (won’t be discussed here), we now discuss parasitic effects *in the interconnect layers*. Again, our goal is to show how these effects can be suppressed through appropriate layout measures.

*The real interconnects are not perfect short-circuits*, in general, there is a line resistance per unit length R`, a line inductance per unit length L`, an insulator capacitance per unit length C`, and an insulator conductance per unit length G` along a conductor. These primary line constants are illustrated as lumped parasitics R, L, C and G in the equivalent circuit diagram for a two-wire conductor in Figure 3.15 (left). The circuit substrate can also assume the role of the second (bottom) conductor.

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Figure. 3.15 Equivalent circuit diagrams for a standard two-wire conductor to illustrate conductor

resistance and inductance, and insulator capacitance and conductance, labeled with the symbols R,

L, C, and G, respectively (left). Also shown are an IC interconnect as RC element (middle) and with

parasitic track resistance (right).

Due to the extremely small dimensions, we can disregard the elf-inductance on a chip as long as the frequencies do not exceed the GHz range. Due to the excellent isolation properties of the oxides, the insulator conductance per unit length is typically negligible as well. On a chip, however, the parasites R and C play important roles (Figure 3.15 middle). (Lienig & Scheible, 2020).

* + - 1. **Line Losses**

In the beginning, we will only take into account the parasitic track resistance R (Fig. 7.13, right), which is determined as follows:

R = R (xx.1)

with line length l, interconnect width w, and sheet resistance R. Thermal loss I2R is caused by this resistance R to the current I flowing in the conductor. Additionally, it results in a potential drop IR in the line, which is the difference between the voltages Vb at the conductor's beginning and Ve at its conclusion. This IR drop must always be taken into account during the routing step.

If the current I is known during layout design, changing R can always change the IR drop. According to Eq. (xx.1), the layout designer can modify the values of line length l, interconnect width w, and sheet resistivity R (depending on the layer selected). IR drops greater than 10 mV should generally be checked at all times. Additionally, the placement of the devices should be optimised in this regard because the line length l greatly depends on the locations of the pins that need to be connected. Therefore, in order to avoid having to make the line width w too wide, devices that have high current flow between them should be placed as close to one another as possible. Generally speaking, the width w should be chosen so that the line's current-carrying capacity is sufficient.

* + - * 1. **Signal Distortions**

Every interconnect on a chip has a significant parasitic capacitance per unit length C to the chip substrate because of the thin deposited layers on the chip. The equivalent circuit diagram in Figure 3.15 (middle) shows a condensed version of this scenario with a lumped capacitance C. For each signal sent through the interconnect, the resistor R (also known as the RC element) must charge the capacitor C. For an ideal step function as the input signal at the line's beginning, see Figure 3.15 (middle). By the time the signal reaches the end of the queue, it has been delayed and distorted. RC, also referred to as the time constant of the RC element, serves as a measure of the time delay (67% of the final value is reached after this time). How can we alter the product R·C in the layout?

The substrate can be thought of as the counter-electrode to each interconnect's capacitor electrode. The well-known parallel plate capacitor equation (xx.2) is as follows:

C = ε0εr (xx.2)

The equation demonstrates that C is inversely proportional to the oxide layer thickness d and scales with the wire surface area A (i.e., with the width w and length l). Because of the lower metal layers' reduced value of d due to their proximity to the substrate, they have higher parasitic capacitances than the upper layers.

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تم إنشاء الوصف تلقائياًBut eq. (xx.2) does not take into account the fringe fields, so it cannot accurately calculate the capacitance of a chip interconnect. (Due to w d and l d, the fringe fields on a typical parallel-plate capacitor are insignificant.) using a chip the lateral fringe fields significantly contribute to C and interconnect. For typical narrow (i.e., small-width) interconnects (e.g., w 2 m for Metal1, w 4 m for Metal2), the capacitance per unit length C fringe resulting from the fringe fields is greater than the plate capacitance per unit length C plate (Fig. 3.16a).

*Figure. 3.16*  Parasitic capacitances between interconnects and the substrate (a); coupling capacitances between interconnects (b); and lateral (c), vertical (d) and all-round (e) interconnect shielding

* 1. **Crosstalk**

A lot of coupling capacitances are produced between laterally adjacent interconnects (Clat) and vertically adjacent interconnects (Cvert) in addition to the capacitances to the substrate (see Fig.3.16 b). These capacitances disrupt the electronic circuit by causing signal crosstalk. The distances between interconnects are getting closer as IC downscaling of feature sizes advances, and these parasitics are getting bigger. Modern Damascene processes can create cross-sections with extremely high and narrow interconnects (Fig. 3.16 c). As a result, *the quantity Clat is more important than Cvert in cutting-edge processes than in traditional processes*. (Lienig & Scheible, 2020).

**The following is a summary of the key principles for physical design crosstalk reduction:**

1. Digital and analog signal isolation: Digital signals typically have sharp edges that contain high frequencies. Due to the AC reactance RC = |1/ωC|, these edges severely perturb capacitively coupled interconnects. Therefore, sensitive analogue signals should be routed apart from digital signals, such as sensor signals. The biggest offenders in this regard are clock nets.
2. Shielding: Crosstalk can be reduced by surrounding interconnects with grounded interconnects if lines cannot be physically isolated or if this isolation is insufficient. As a result, the lines are protected from disruptions. The three shielding configurations are: all-around, all-lateral, and vertical only (see Fig. 3.16c-e).
3. Avoiding minimum spacings: The lateral interconnect spacing within a layer can be changed, whereas the ILO (interlevel oxide) thickness cannot be. If the footprint permits, it is a good idea to forgo using minimum spacings for crucial interconnects (both for perpetrators and victims). It is best practice to use any remaining whitespace after routing all nets to increase or decrease wire spacing.

**3.6 Latch-Up**

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path. CMOS circuits use NMOS and PMOS transistors to create the circuit functions. In the design of the CMOS integrated circuit, the proximity of the PN junctions that form the NMOS and PMOS transistors create inherent parasitic transistors and diodes. These parasitic structures create PNPN Thyristors, also called silicon-controlled rectifiers (SCRs). Excursions (overshoots and undershoots) outside the normal operating voltage and current levels can trigger PNPN Thyristors and may cause Latch-Up. Latch-Up is not a risk if the voltage and current levels applied to the device adhere to the absolute maximum ratings.

**صورة تحتوي على رسم بياني, خطة, رسم تقني, خط

تم إنشاء الوصف تلقائياً**The parasitic thyristor structure that causes latch-up is formed due to the interactions between the PNP and NPN bipolar transistors that are present in the integrated circuit. When the voltage across the base-emitter junction of the PNP transistor exceeds a certain threshold, a parasitic NPN transistor is formed between the PNP collector and the NPN base. Similarly, when the voltage across the base-emitter junction of the NPN transistor exceeds a certain threshold, a parasitic PNP transistor is formed between the NPN collector and the PNP base. Once these parasitic transistors are formed, they can conduct current between the power supply rails, leading to latch-up , see figure 3.17. [11]  
 Figure 3.17 Parasitic Transistors in a CMOS Circuit

Latch-up is a significant problem in analog circuit layout design, as it can cause damage to the circuit and lead to circuit failure. It is caused due to the interaction of parasitic transistors that are inherent in the layout of a standard CMOS transistor. When the circuit is powered up, the parasitic transistors interact with each other, creating a feedback loop that can cause the circuit to lock up in a conducting state. The excess current creates heat, which can cause damage or even destroy the circuit. Latch-up is an important consideration in analog circuit layout design, and careful attention to the layout and component placement can help avoid the problem and ensure a reliable and robust circuit. It's important to note that latch-up is not specific to analog circuits and can occur in digital circuits as well. However, the effects of latch-up in digital circuits are generally not as significant as in analog circuits. For example, in digital circuits, the latch-up may cause a delay in switching, but it is unlikely to cause damage to the circuit. [[[11]](#footnote-11)]

**3.6.1 Latch Up types**

1. **Undershoot latch-up** refers to a type of latch-up that occurs when a voltage undershoot (a temporary decrease in voltage) triggers an internal parasitic bipolar transistor in a CMOS circuit. During undershoot latch-up, the substrate diode of the parasitic transistor becomes forward-biased and conducts, causing a large current to flow through the device. This can lead to the device getting stuck in a high-current and potentially destructive state until the power supply is turned off. Undershoot latch-up can happen in a variety of situations, such as when there is a sudden decrease in the power supply voltage, when the circuit is subjected to electromagnetic interference (EMI), or when there is a large current flowing through the circuit. The risk of undershoot latch-up can be mitigated through proper design techniques such as using guard rings and designing a well-balanced layout. [12]
2. **Overshoot latch-up** as a type of latch-up that can occur in certain situations. Overshoot latch-up can occur when a voltage overshoot (a temporary increase in voltage) triggers an internal parasitic bipolar transistor in a CMOS circuit. The overshoot may cause a high voltage to be applied to the gate of the parasitic transistor, causing it to become forward-biased and conductive. As a result, a large current can flow through the device, leading to latch-up. Overshoot latch-up is a less common type of latch-up compared to undershoot latch-up, but it can still occur in certain situations, for example when there is a sudden increase in the power supply voltage, or when the circuit is subjected to electromagnetic interference (EMI). Proper design techniques such as guard rings and a well-balanced layout can also help reduce the risk of overshoot latch-up . [[[12]](#footnote-12)]

**3.6.2 Latch up Prevention**

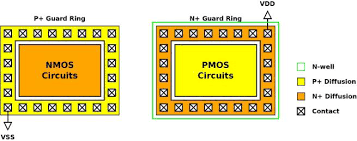
Latch-up is often caused by design flaws rather than manufacturing defects. It can be avoided by proper layout design, which involves placing critical components in specific locations and taking into account the parasitic effects of the components. Simulation tools can be used to predict and analyze the behavior of the circuit and identify potential latch-up conditions before the physical layout is created. Additionally, Spacing of the elements of each transistor, diode, resistor and capacitor are now being controlled through process characterization and design rules to help minimize the effect of current or voltage pulses on the products. Additionally, guard rings have been added around known radiators in the circuits or if spacing concerns are critical around individual PMOS and NMOS transistors, diodes or substrate resistors. Guard rings act as injected carrier syphons allowing these carrie rs to flow to the supply or ground. Also, the use of substrate ties and well taps act as excited carrier syphons and are guided by design rules for placement. These ties and taps are necessary for Latch-Up immunity.

figure 3.18 Guard Rings in a CMOS Circuit

Another very effective method of quenching Latch-Up is to use an EPI (epitaxial silicon) layer. The EPI layer is doped appropriately for the best transistor performance (more lightly doped than the remaining lower portion of the substrate that is highly doped). The highly doped substrate directs majority carriers to ground and reflects minority carriers making the guard rings more effective (see Figure 2). Even with these safeguards, there is a possibility of parasitic transistors in circuits that are not identified. These unidentified Latch-Up sources need to be identified; one way is a Latch-Up stress test.

In conclusion, avoiding latch-up is essential for the successful design and performance of analog circuits. Careful layout design, modeling, and simulation can help identify potential latch-up conditions and prevent them. Additionally, testing and validation ensure that the final design is robust, reliable, and meets the required specifications .

**3.6.3 Latch-Up Test**

Latch-up test circuits are used to test the susceptibility of integrated circuits (ICs) to latch-up, The latch-up test circuit is designed to simulate the conditions that can cause latch-up in an IC. It consists of a power supply, a voltage source, and a current source. The power supply provides the voltage and current necessary to activate the parasitic transistor. The voltage source is used to apply a voltage to the IC, while the current source is used to apply a current to the IC , see Figure( 3.19) The test circuit is connected to the IC under test and the power supply is turned on. The voltage source is then adjusted to the desired level and the current source is adjusted to the desired level. The voltage and current levels are then monitored to ensure that they remain within the specified limits. If the voltage or current levels exceed the specified limits, the test circuit is shut off and the IC is examined for any صورة تحتوي على رسم بياني, رسم تقني, خطة, رسم

تم إنشاء الوصف تلقائياًsigns of latch-up.

figure 3.19 Latch-Up Test Circuit

The latch-up test circuit is an important tool for ensuring the reliability of ICs. It can help identify potential problems before they become serious, and can help prevent costly failures. It is also important to note that the test circuit should be used in conjunction with other tests, such as thermal testing, to ensure that the IC is functioning properly.

**3.7 Electro migration (EM**) [[[13]](#footnote-13)]:  is one of the major challenges faced by electronic circuit designers in layout. It can occur in areas where high electric currents pass through long wires containing fine conductors.it can damage interconnect

wires, vias , metals which because of big current density which electrons in the wires and metals moved with high acceleration

صورة تحتوي على لقطة شاشة, مستطيل, أسود وأبيض, أسود

تم إنشاء الوصف تلقائياً

There are several solutions to mitigate the effects of electromigration in electronic circuit layout [[[14]](#footnote-14)], such as:

* Use wider metal tracks: Increasing the width of the metal tracks can reduce the resistance and increase the current carrying capacity, reducing the likelihood of electromigration.
* Use lower current densities: Limiting the current density in the metal tracks can reduce the likelihood of electromigration. This can be achieved by using thicker metal tracks or by reducing the current passing through the tracks.
* Use shorter connection paths: Reducing the length of the metal tracks can decrease the time the current flows through the conductors, reducing the likelihood of electromigration.
* Use copper instead of aluminum [[[15]](#footnote-15)]: Copper has better resistance to electromigration than aluminum, so using copper interconnects can reduce the likelihood of electromigration.
* Improve the thermal management of the circuit: By reducing the temperature of the circuit, the likelihood of electromigration can be reduced. This can be achieved by optimizing the layout to reduce heat generation, or by using cooling techniques such as heat sinks or fans.
* Use simulation and testing: Simulation tools can be used to model the performance of the circuit and identify potential issues related to electromigration.

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